Dependable System Design For Reconfigurable Safety-Critical Applications

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Research Group: CAD group

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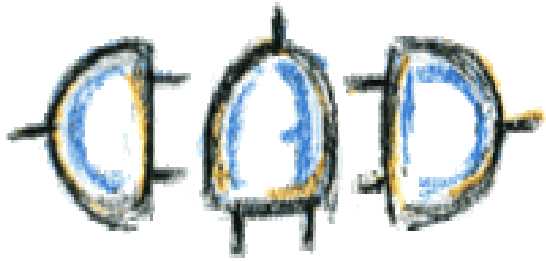


Outline

- Dependability
- Re-configurability
- FPGA architecture and Slice Internals
- Problem Statement and goal
- Fine-grain Self-Repairing System (FGSR)
- Dynamically Reconfigurable TMR (DrTMR)
- ASIC fault emulation (FE)
- Conclusions
- Future Work

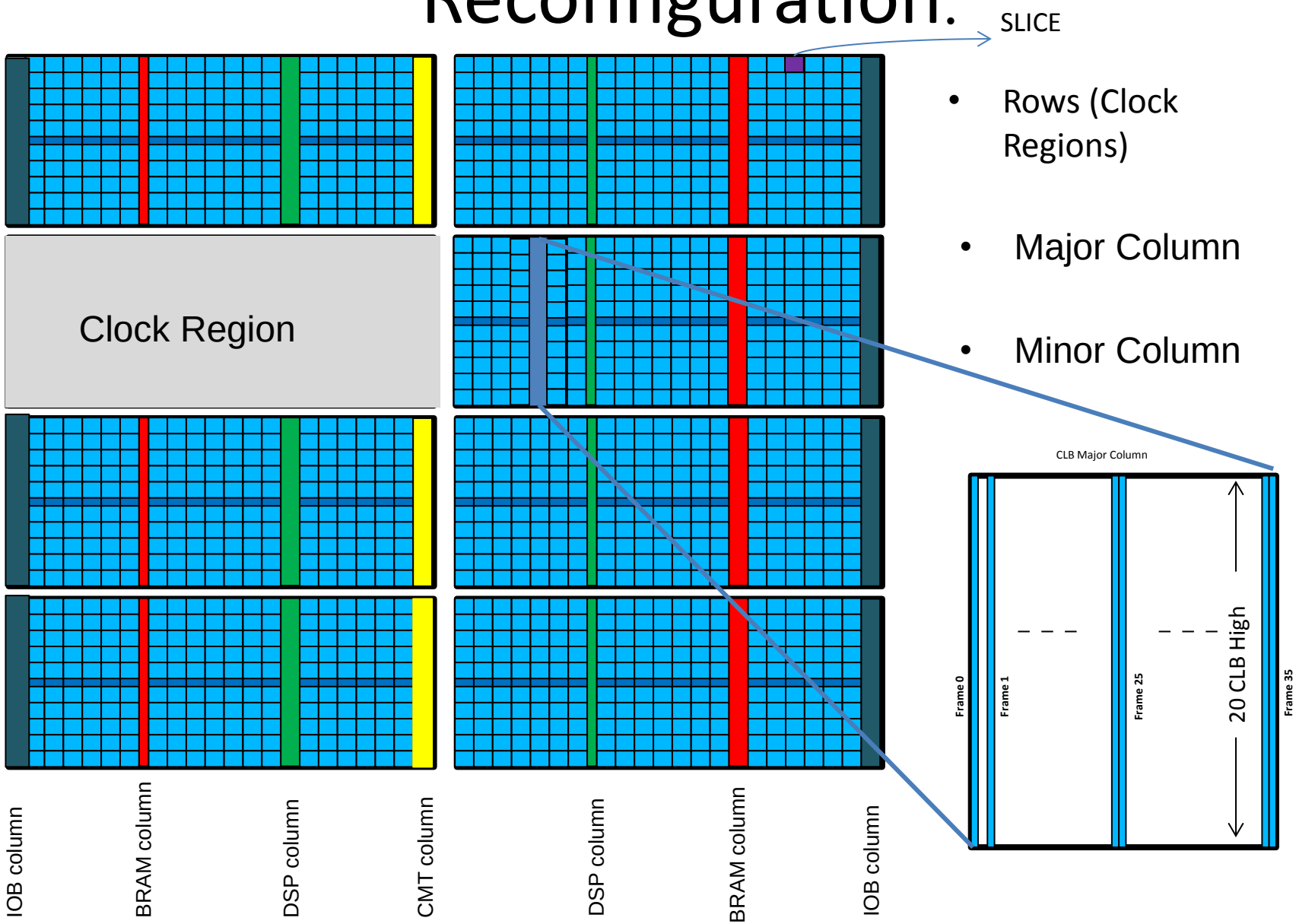
Dependability

- Reliable computations in today's Nano-metric technology is challenging
  - Manufacturing defects *(stuck-at, stuck-open, bridge faults)*
  - In-operational effects *(radiations , electro-migration, aging)*
- Dependable system design techniques should be applied from RTL to implementation phases
- These mitigation strategies are assessed with testing and *fault injection* techniques to ensure the desired reliability levels are attained

Re-configurability

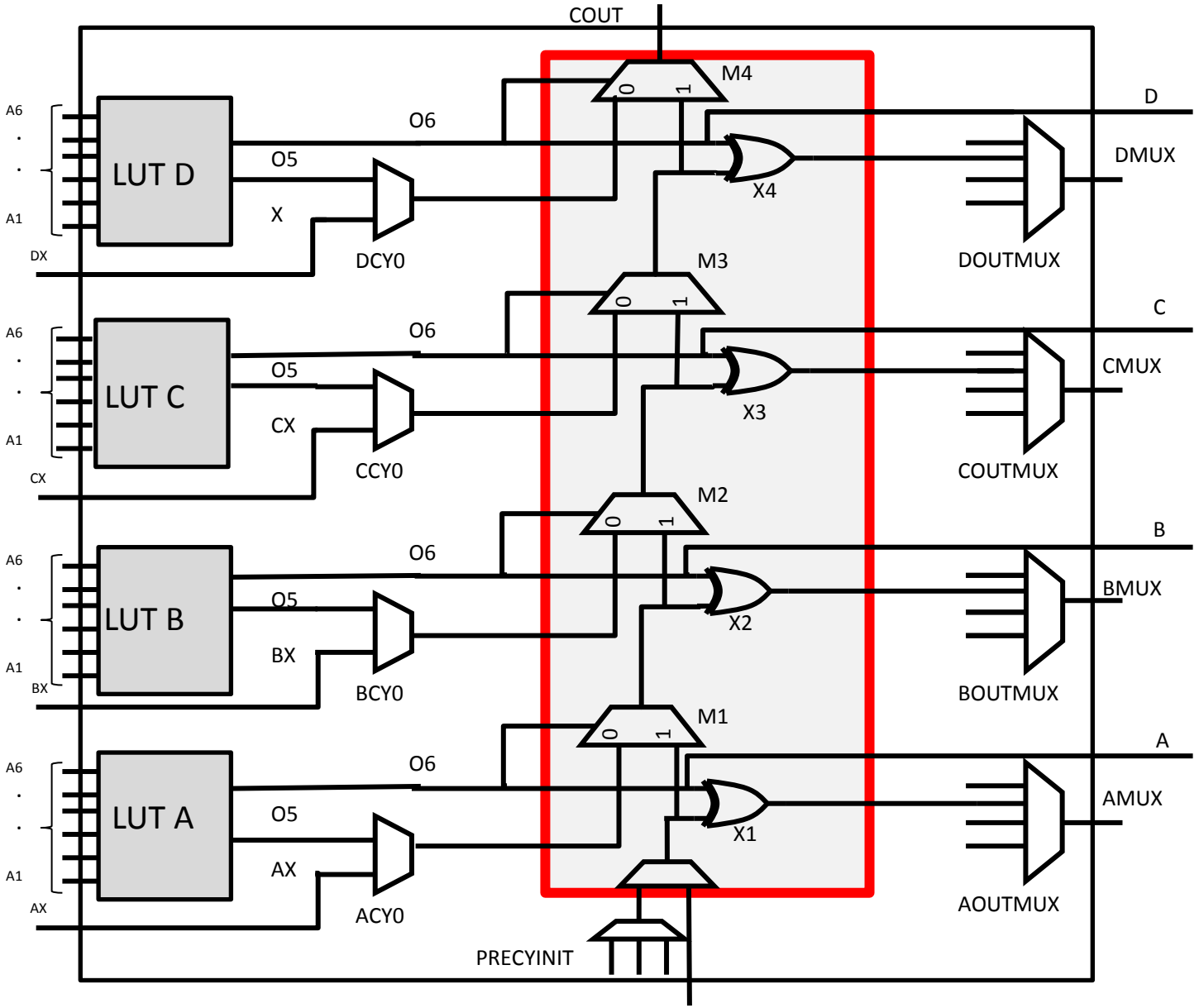
- FPGAs are electronic devices that can upgrade and change its functionality *in-field*
- *Redundancy* for error masking/detection combined with *re-configuration* for correction is used in critical system design
- Re-configurability can also be used for fault injection/emulation as a tool of dependability *assessment*
- SRAM-based FPGAs are highly sensitive to *Soft Errors* and have huge *recovery times*

SRAM-based FPGAs: architecture & Reconfiguration.



- Rows (Clock Regions)
- Major Column
- Minor Column

FPGA's Slice Architecture



Problem statement and Goal

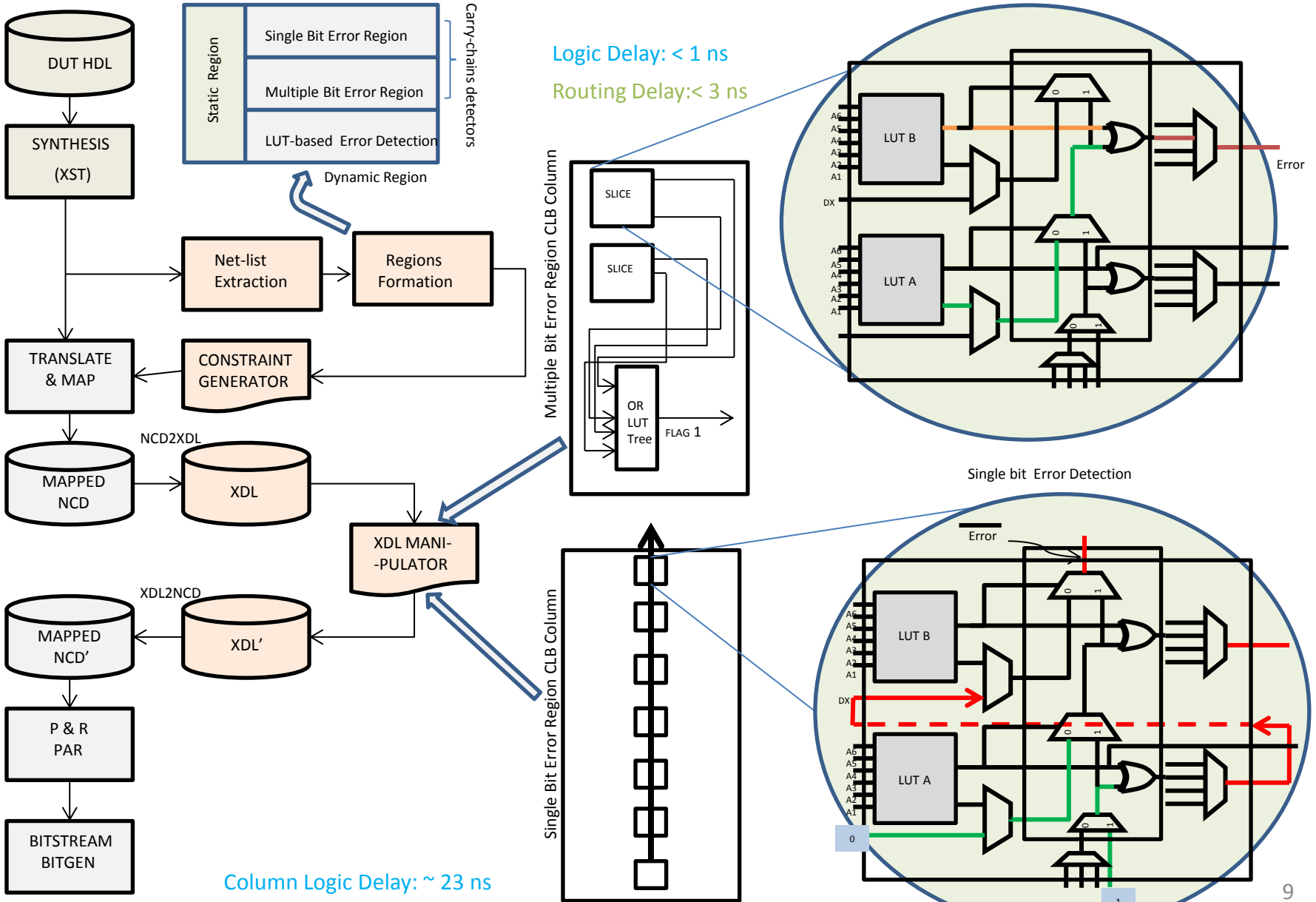
- To mitigate the effects of *Multiple Bit Upsets (MBUs)* in the configuration memory and reduce the *recovery* times
- Fine-grain redundancy offers better mitigation properties, precise diagnosis of faults and fast error detection while fine-grain reconfiguration improves the recovery times
- The *challenge* is the overhead introduced by fine-grain approaches and the lack of design tools and methodologies
- The *goal* of this work is to exploit the FPGA's primitive elements (LUT, carry-chains) to support fine-grain approaches to redundancy and reconfiguration

Fine-grain self-repairing (FGSR)

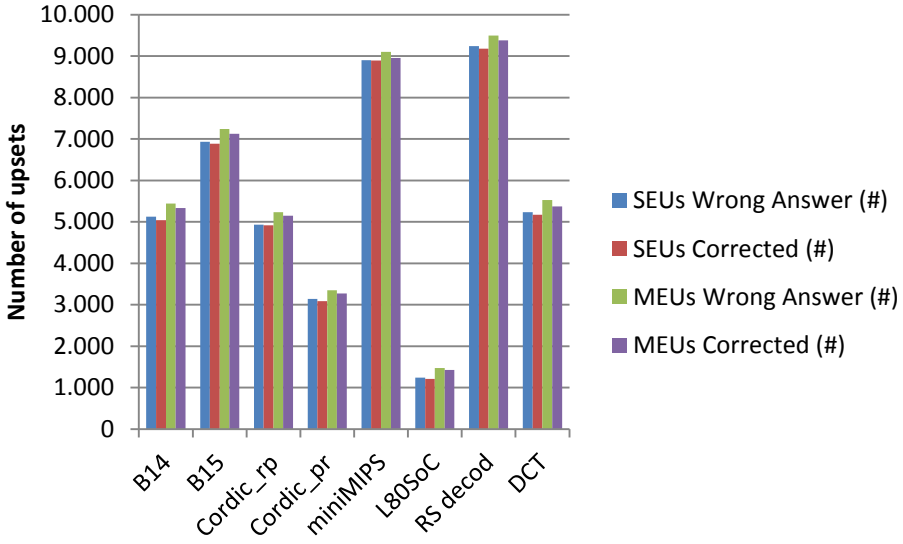
- Self-repairing systems contain a Static and a Dynamic region implemented on a reconfigurable platform
- The Static region consists of resources *(processors, memories, I/O interfaces)* that are always required for the operation of the system
- The Dynamic region contains reconfigurable modules that can change functionality during operational phase of the system called *Partial Reconfigurable Modules* (PRMs)
- The research aim is to increase the fault tolerance capabilities for PRMs with reliable and fast error-detectors having a low area-overhead

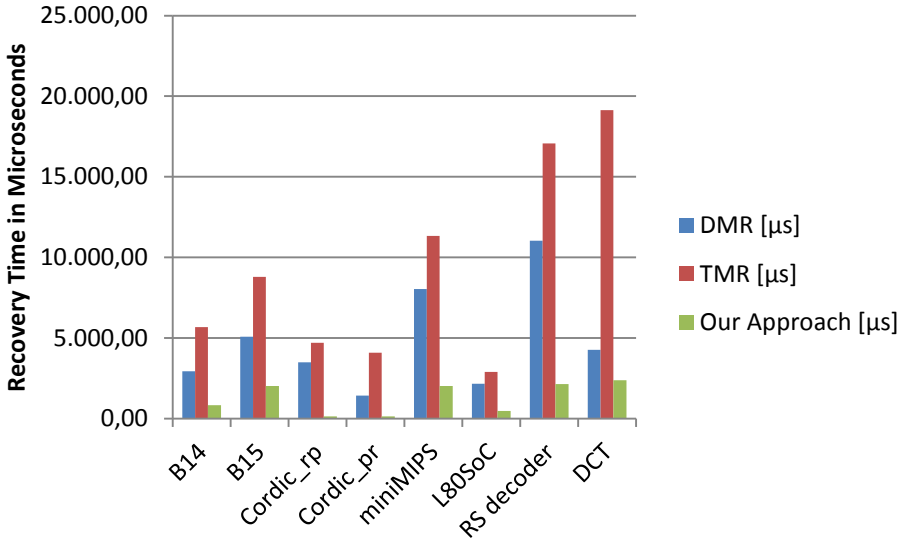
Matteo Sonza Reorda, Luca Sterpone and Anees Ullah, "**An Error-Detection and Self-Repairing Method for Dynamically and Partially Reconfigurable Systems",** *in IEEE European Testing Symposium (ETS 2013), May 27-31, 2013 (extended version submitted to IEEE Transaction on Computers)*

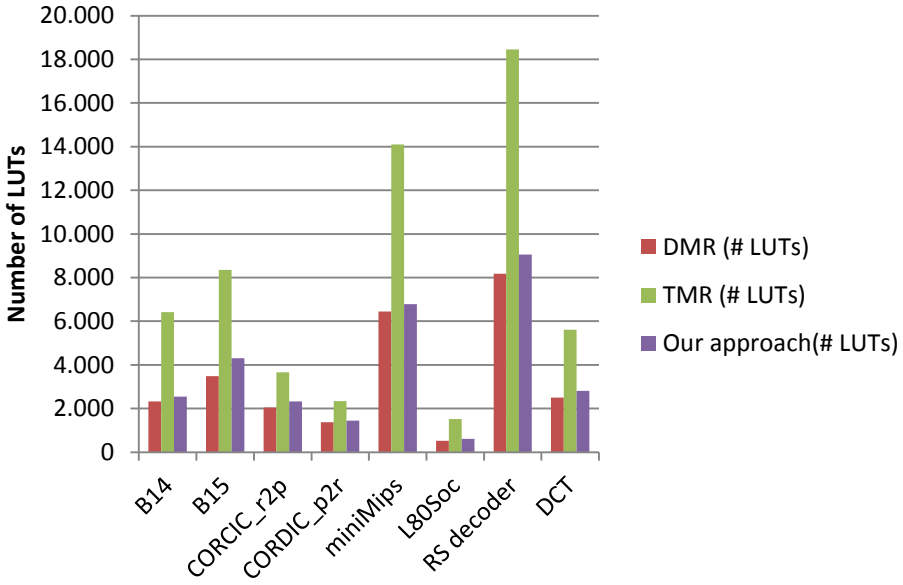
FGSR - Methodology

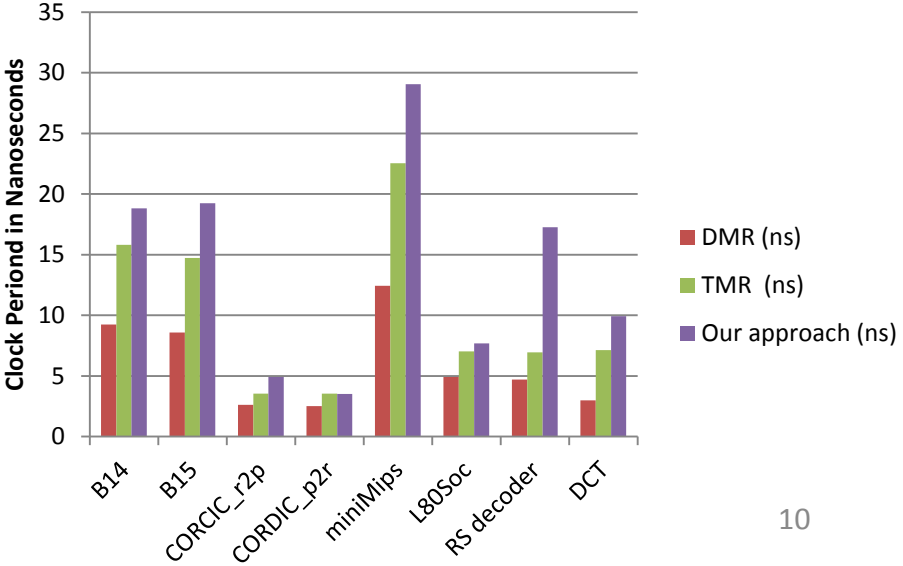


FGSR - Results



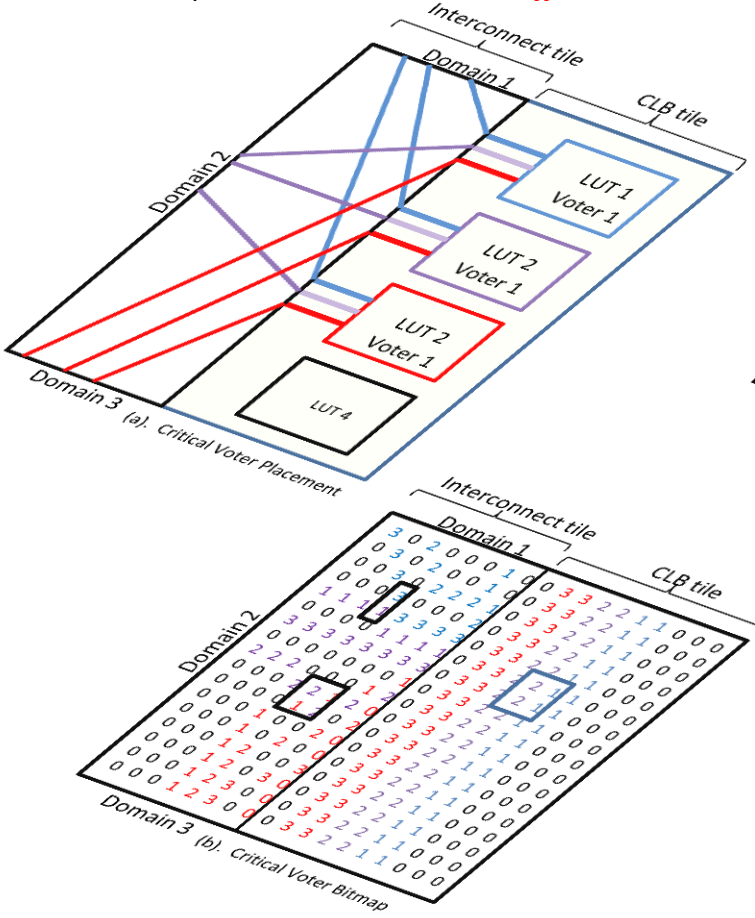




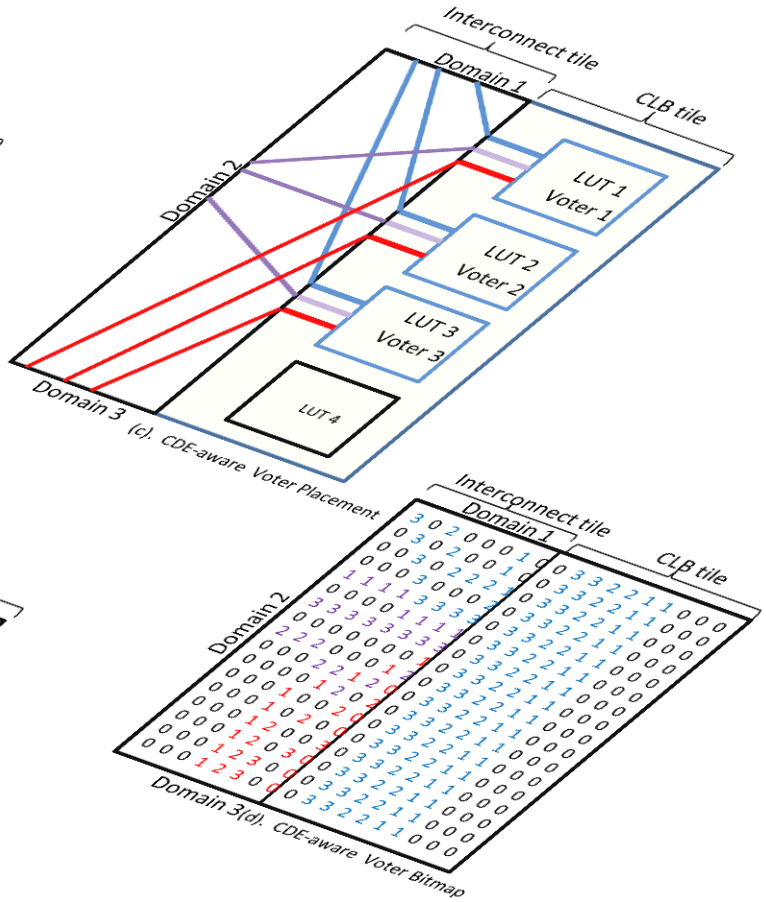


Dynamically Reconfigurable TMR (DrTMR)

Critical-Voter placement - Voters from *different* Domain in a Slice



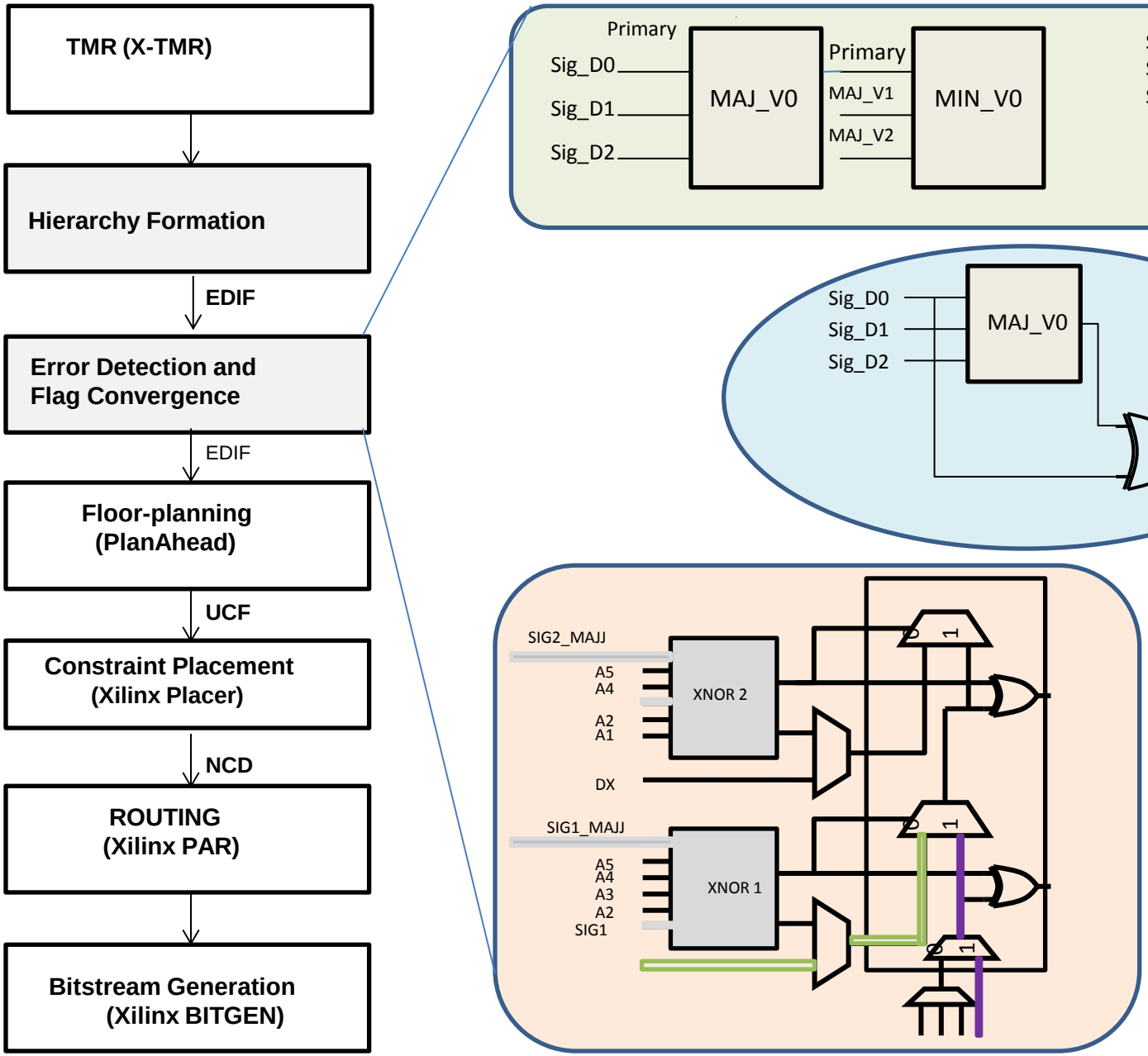
CDE-aware Voter placement - Voters from *same* Domain in a Slice



Mixed placement of TMR domain *increases* the probability of Cross Domain Errors and makes partial Reconfiguration of TMR domains *impossible*

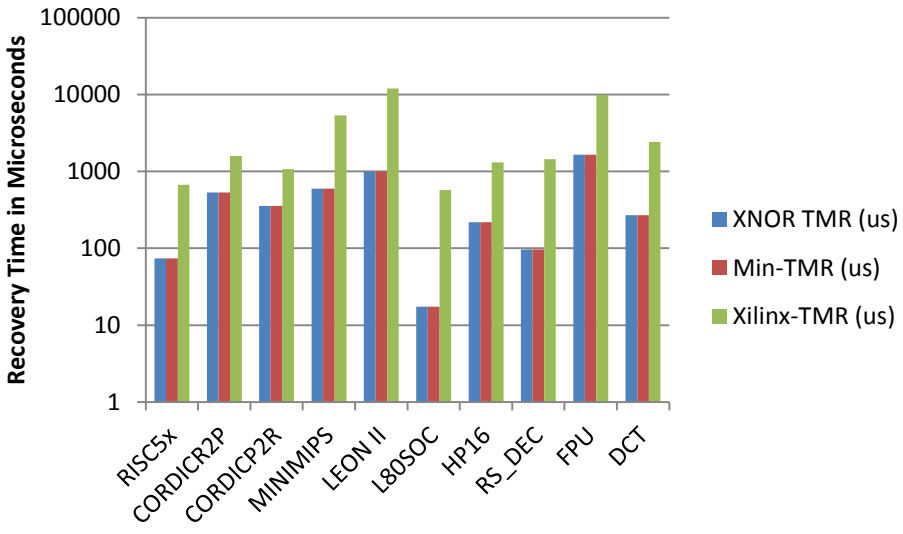
1. **"On the Optimal Reconfiguration times of TMR circuits on SRAM based FPGAs"**, *in IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2013), June 25-27, 2013*
2. **Real-Time SEU Tolerant Circuits on SRAM-based FPGAs"**, *in 2013 IEEE Convention on Radiation Effects on Components and Systems (RADECS 2013) , Sep 23-27, 2013*
3. **"Recovery Time and Fault Tolerance Improvements for Circuits mapped on SRAM based FPGAs",** *Journal of Electronic Testing: Theory and Applications (JETTA)*

DrTMR - Methodology

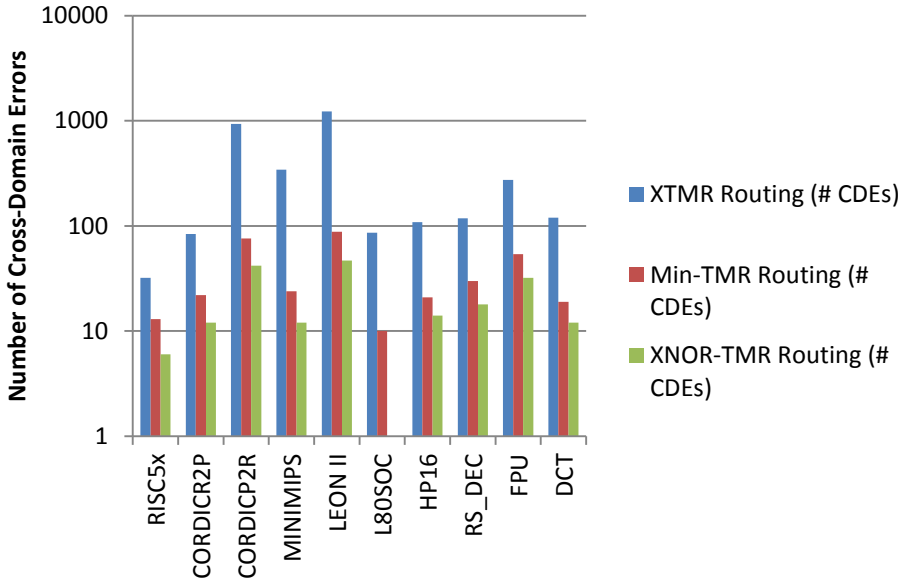


DrTMR - Results

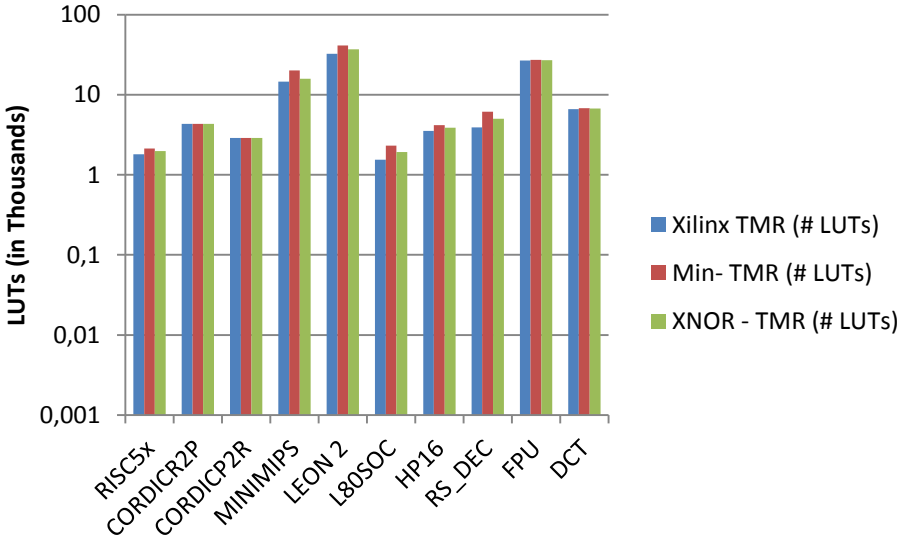
Error Latency = 28 ns @ 192 CLBs

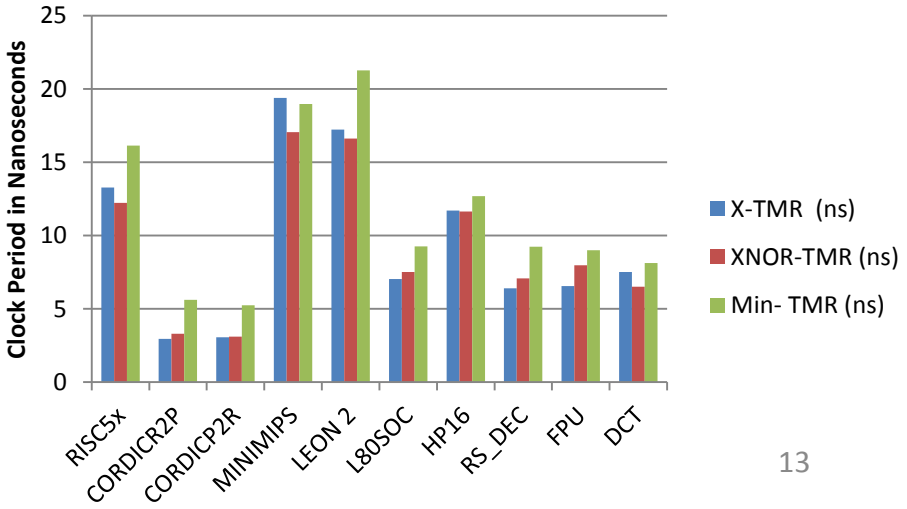


Zero CDEs in Logic



1 LUT per Majority Voter



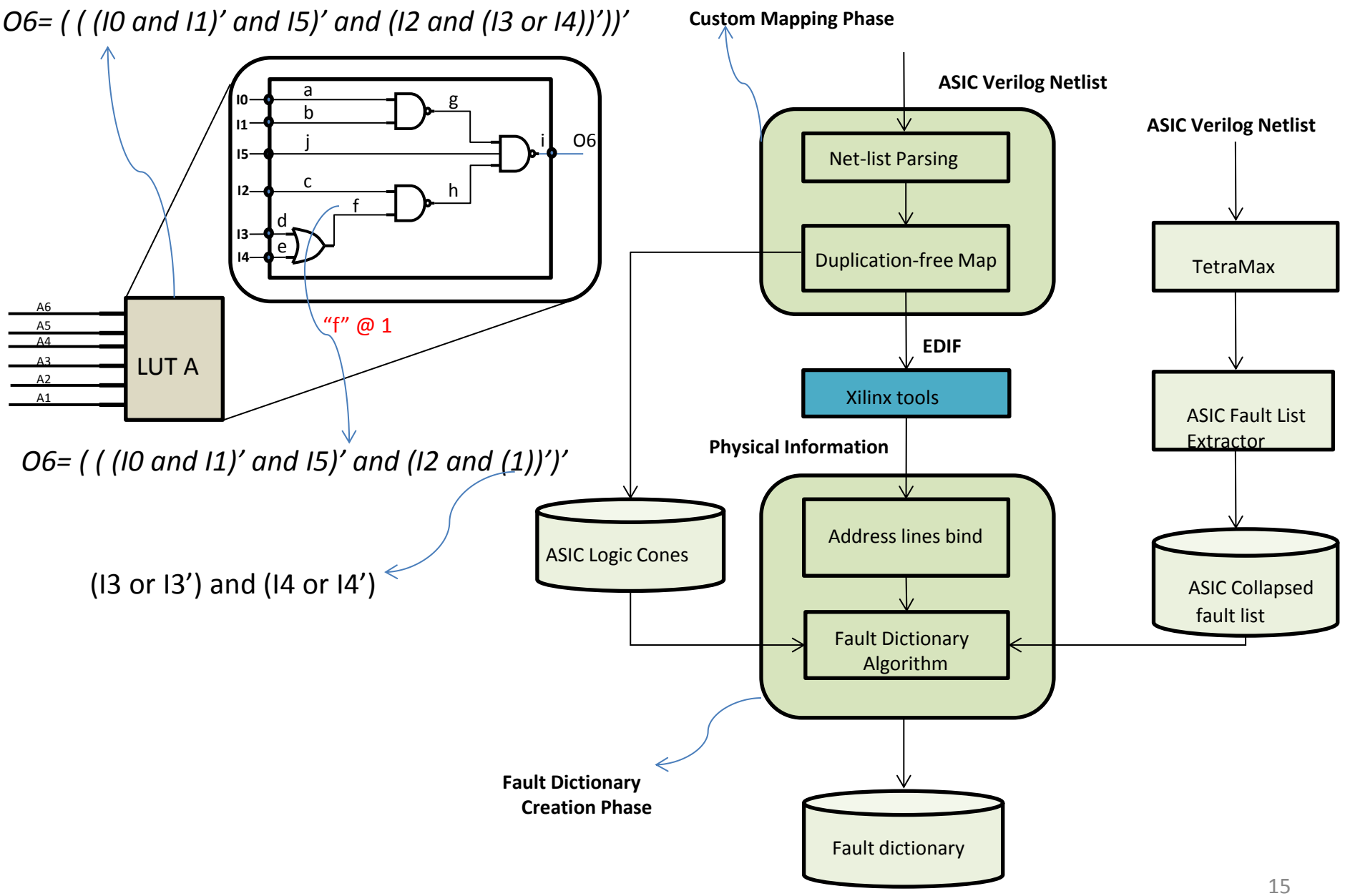


ASIC Fault Emulation (FE)

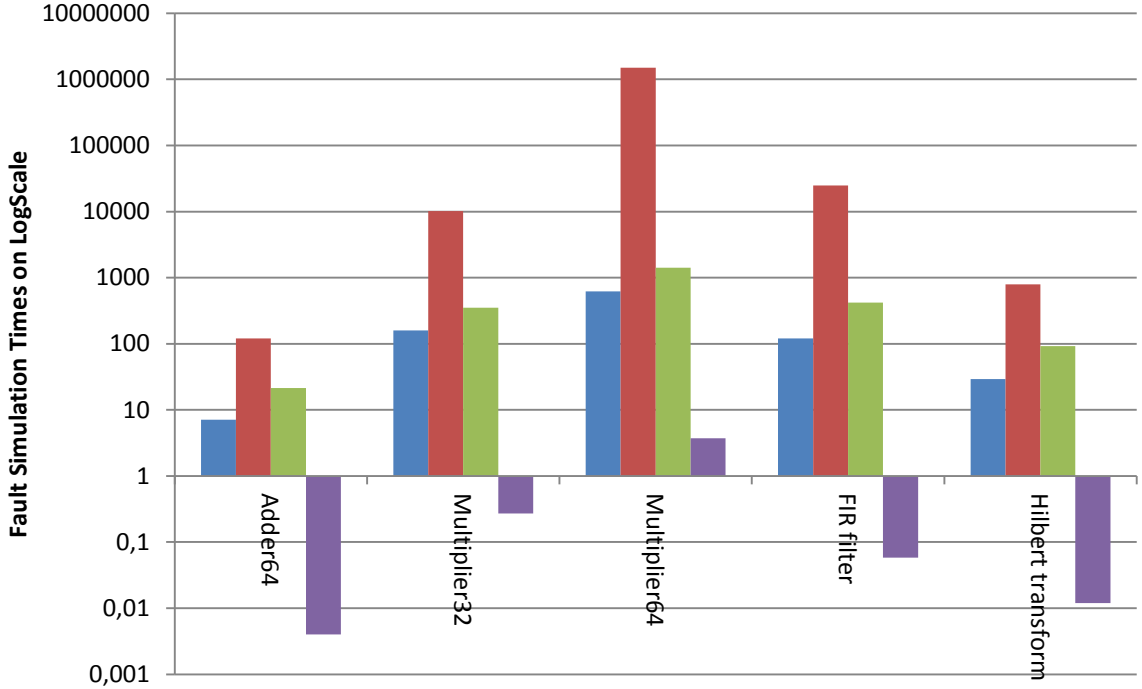
- The simulation of a circuit in the presence of faults is called fault simulation and it is a mandatory step to determine the *yield* of any VLSI fabrication process
- Fault Emulation is the hardware realization of fault simulation process in order to achieve *speed*
- The research aim of this activity is to exploit the *flexibility of LUTs* for fault injection purposes; emulating the ASIC *permanent* faults on FPGA

"**Effective emulation of permanent faults in ASICs through Dynamically Reconfigurable FPGAs** *", in 24th IEEE International Conference on Field Programmable Logic and Applications Munich, Germany; September 2 - 4, 2014*

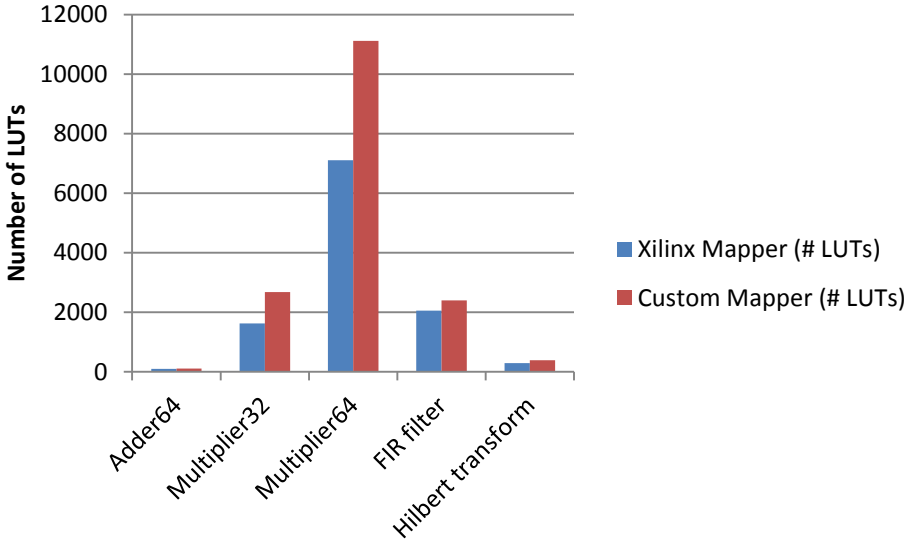
FE - Methodology

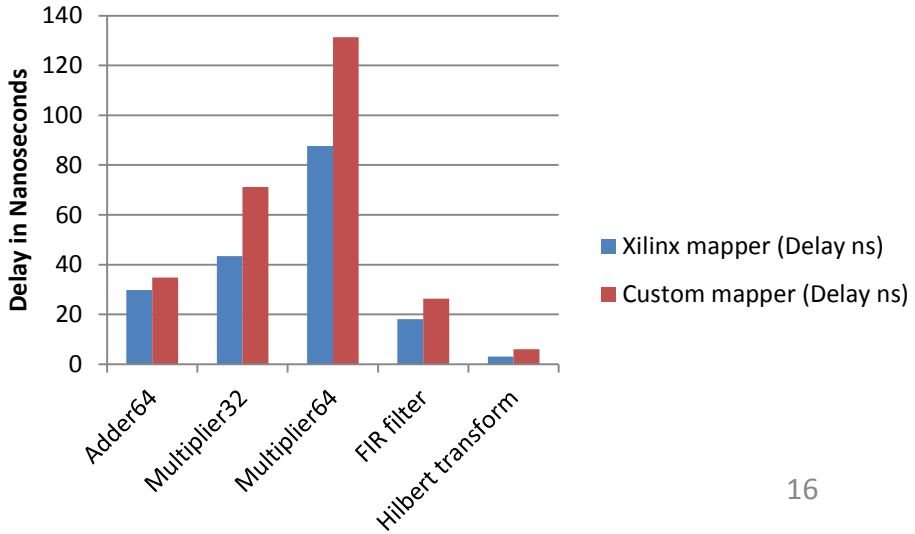


FE - Results



No re-compilation
Guaranteed emulation





Conclusions

- The fine-grain approaches to reconfiguration and redundancy *simultaneously* improves the fault tolerance and reconfiguration times

- These improvements are achieved at an *affordable* area and clock period overhead

Future Work

- As future a work, *radiation testing* of the developed mitigation techniques need to be conducted

- The developed *CAD algorithms* can be be optimized with respect to clock period, area and reconfiguration times

Questions?

Thank you!